Controller Design and Real-time Implementation

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Abstract: This project studies the design and implementation of a real-time control system with the use of Simulink, xPC Target, and a Stamped Circuit Board (SCB). A continuous time system is discretized and a discrete time controller is designed to have the system meet required specifications. The specifications are on such system dynamics as stability, steady state error, settling time, and maximum overshoot. A proportional controller (K) proved efficient and a model of the system was simulated using Simulink. From this simulation, a desired range for K was created. The system was then implemented in real-time through the use of xPC Target and SCB. Due to circuit signal noise from the SCB, a new desired range for K was created. From this new range, an ideal value for K is chosen based on the tradeoff that exists between the settling time and maximum overshoot of the system.

CIT-Labs

Introduction*

It was required to master the programming language of Simulink before a controller could be designed and implemented on a physical model. Additionally, for real-time controller implementation, running parallel with Simulink is a software known as xPC Target. Similar to learning Simulink, there needed to be some level of comfort with xPC Target before the controller could be tested in real-time. Lastly, knowledge of SCB (Stamped Circuit Board) circuitry was needed to implement the controller in real-time. The SCB also needed to be appropriately wired based on the model of the physical system and to prevent hardware damage.

For simplicity, the plant $G(s)$ used in the experiment has a continuous time transfer function of:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{s}$$

Continuous Time Transfer Function (Continuous Time Plant)

In this experiment, there were specifications on stability, steady state error, settling time, and maximum overshoot.

Specifications

Depending on the given specifications, the system will exhibit both desired and undesired behavior. If there exists any undesired behavior in the physical system, a controller must be implemented to achieve the specifications. The specifications self-enforced on the system are as follows:

- The system should be stable
- 0 steady state error to a unit step input
- A setting time of less than 2 seconds
- And an overshoot less than 5%

Based on the form of the continuous time transfer function, it is hypothesized that a proportional controller will meet all the specifications described above.

Method

The system was tested using Simulink and xPC Target to verify that the specifications have been successfully satisfied. First, a model of the system was created in Simulink without any “real-time” blocks, such as the PCI-6259 Analog Input/Output. The simulation results show that the controller design efficiently produced desired closed loop behavior. This allowed for the construction of a desired range for the gain K that met the specifications. Next, the PCI-6259 Analog Input/Output blocks were appropriately placed in the previous block diagram. The output of the controller was limited to a value of ten to prevent damage to lab equipment. Thus, the results of the real-time model differ from the results of the simulation, and a new desired range for the gain K that met the specifications was formed.

* Through the projects development, it was appropriate for a collection of tutorials to be devised for future project members. The tutorials are uploaded onto the project team’s Cornell Box and their exact location within the Cornel Box can be found on the project Wiki page at https://sites.google.com/a/cornell.edu/ssds/projects/eddy-current-page/weekly-reports.

Discretizing the System

When controllers are digitally implemented, it is important to discretize the continuous time transfer function into $G(z)$before meeting the specification requirements:

$$G(z) = \frac{Y(z)}{U(z)}$$

Discrete Time Form

Additionally, an appropriate sampling rate (T) must be used in conjunction with the discrete time system. A good standard in developing the sampling rate is that it should be two orders of magnitude faster than the system dynamics. The continuous time controller will result in one discrete time pole located at $z = 1$. Since there is only one pole with magnitude 1, the appropriate sampling rate is given as:

$$T = .01$$

Sampling Rate

The first step in discretizing the plant is to develop a state space representation for the continuous time system as so:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1 \cdot z}{s \cdot z}$$

Equation 1

Equation 1 yields the following two equations:

$$y(z) = z$$

Equation 2

$$u(z) = \dot{z}$$

Equation 3

Letting x_1 denote z and $\dot{x_1}$ denote $\dot{z}$, the state space representation is:

$$\dot{x_1} = u \qquad y = x1$$

Continuous State Space Representation

Therefore, the A and D matrices are found to be 0, while the B and C matrices are found to be 1. This continuous time state space representation can be converted to discrete time using the difference equation:

$$x(k+1) = \varphi x(k) + \gamma u(k) \qquad y(k) = x(k)$$

Discrete Time State Space Representation in Variable Form

Where φ is given by e^{AT} and γ is given by $\int_0^T e^{A\tau}\,d\tau$. Plugging in the appropriate numbers for φ and γ:

$$\varphi = e^{AT} = e^{(0)(.01)} = e^0 = 1$$

Equation 4

$$\gamma = \int_0^T e^{A\tau}\,d\tau = \int_0^{.01} e^{(0)\tau}\,d\tau = \int_0^{.01} d\tau = .01$$

Equation 5

After plugging in the values obtained in Equations 4 and 5, the difference equation reads:

$$x(k+1) = 1x(k) + .01u(k) \qquad y(k) = x(k)$$

Discrete Time State Space Representation

The next step in the discretization process is to apply the Z-transform on the difference equation as so:

$$zX(z) = 1X(z) + .01U(z) \qquad Y(z) = X(z)$$

Z-Transform

These two equations can be solved to eliminate $X(z)$ and solve for $G(z)$ (as defined by the *Discrete Time Form)* in terms of z. Since the equation on the right shows that Y(z) = $X(z)$, $Y(z)$ can replace $X(z)$ in the equation on the left giving:

$$zY(z) = 1Y(z) + .01U(z)$$

Equation 6

Solving for $G(z)$ yields the discrete time transfer function:

$$G(z) = \frac{Y(z)}{U(z)} = \frac{.01}{z-1}$$

Discrete Time Transfer Function (Discrete Time Plant)

0 steady state error

To satisfy this specification, a proportional controller (K) is implemented on the system and the Final Value Theorem is used on $E(z)$, the error for this transfer function.

The transfer function of the error for this model is given by:

$$\frac{E(z)}{R(z)} = \frac{1}{1 + G(z)K} = \frac{1}{1 + \frac{.01}{z-1}\,K}$$

Transfer Function of the Error

Where $R(z)$ is a unit step input and is given by:

$$R(z) = \frac{Tz}{z-1} = \frac{.01z}{z-1}$$

Unit Step Input

The transfer function of the error simplifies to:

$$\frac{E(z)}{R(z)} = \frac{z-1}{z-1+.01K}$$

Transfer Function of the Error

The general form of the Final Value Theorem for a discrete time system is given as follows:

$$e(\infty) = \lim_{z \to 1}(z-1)E(z)$$

Final Value Theorem

From the transfer function, after plugging in $R(z)$, $E(z)$ can be found to be:

$$E(z) = \frac{z-1}{z-1+.01K}\,R(z) = \frac{.01z(z-1)}{(z-1)(z-1+\ .01K)}$$

Equation 7

In applying the Final Value Theorem to $E(z)$ in Equation 7, the steady state error is calculated as:

$$e(\infty) = \lim_{z \to 1}(z-1)\,\frac{.01z(z-1)}{(z-1)(z-1+.01K)} = \lim_{z \to 1}\frac{.01z(z-1)}{(z-1+.01K)} = \ 0$$

Evaluation of the Final Value Theorem

An important property of the Final Value Theorem is that the transfer function in question must be stable. In discrete time, a system is unstable if the poles are located outside of the unit circle. The system is stable if the poles are located within the unit circle. Those poles which can be found exactly on the unit circle are considered marginally stable. Without the presence of the proportional controller, the system is marginally stable in having a pole at +1 (on the unit circle). Since the root locus will move the pole to the left, an infinitesimal value greater than 0 will make the system stable. Therefore, there will be a maximum value for K, the value at which the pole can be located on the opposite end of the unit circle at -1. Hence, the stability and 0 steady state error requirements are satisfied with a proportional controller having a specific range for K. The open loop discrete system is given by:

$$G(z)K = \frac{.01K}{(z-1)}$$

Open Loop Discrete Time System

Figure 1 shows the root locus plot of the open loop discrete time system:

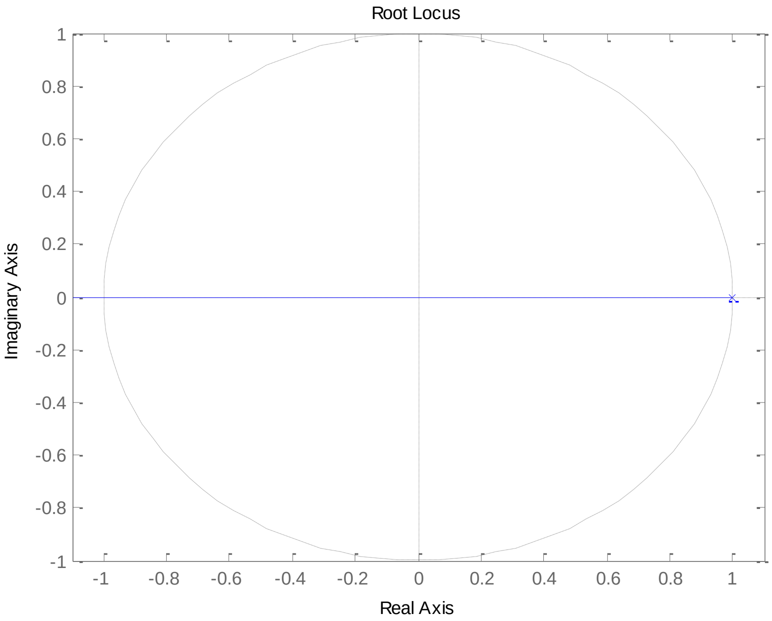

Figure 1

In labeling the points of marginal stability in Figure 2, the desired range for the gain K is evident:

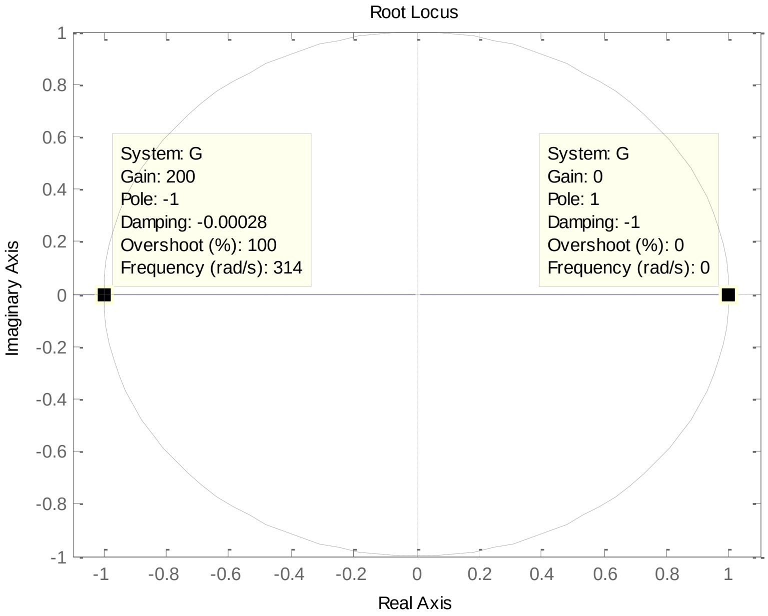

Figure 2

From the root locus plot in Figure 2, the range of K for stability and 0 steady state error is given by:

$$0 < K < 200$$

Range for K Meeting the Stability and Steady State Error Specifications

Although this range will satisfy the stability and 0 steady state error specifications, it does not take into account the settling time or overshoot specifications. It is hypothesized that the current range for K will need to be reduced to fulfill all four of the specifications.

Settling Time Less Than 2 Seconds

The root locus of the open loop discrete system is also a useful tool in visualizing the settling time. The settling time specification can be viewed as an inner circle with radius:

$$z \leq e^{-\text{ב}\,\omega nT}$$

Discrete Time Settling Time Equation

Where $\text{ב}\omega n$ is obtained from the settling time specification (t_s) in the continuous time S-plane using the 2% criterion:

$$t_s < \frac{4}{\text{ב}\omega n} < 2$$

S-plane Settling Time Equation

In solving the S-plane settling time equation for $\text{ב}\omega n$, the following equation is obtained:

$$\text{ב}\omega n > 2$$

Equation 8

As stated earlier, the sampling rate (T) in use on this system was .01. In applying these values to the settling time formula in the Z-plane, the following radius is obtained:

$$z \leq e^{-\text{ב}\,\omega nT} \leq e^{-2(.01)} \leq .9802$$

Evaluation of the Settling Time Equation

In order for the settling time specification to be satisfied, the poles must be located within the circle of radius .9802 measured from the origin. Since there is one pole at exactly +1.0, and given that the root locus for that pole only moves towards the left, there is a minimum value for K that satisfies the settling time specification. Likewise, there will also be a maximum value for K that satisfies the settling time specification. The range for the desired K can be found using the root locus of the open loop discrete system:

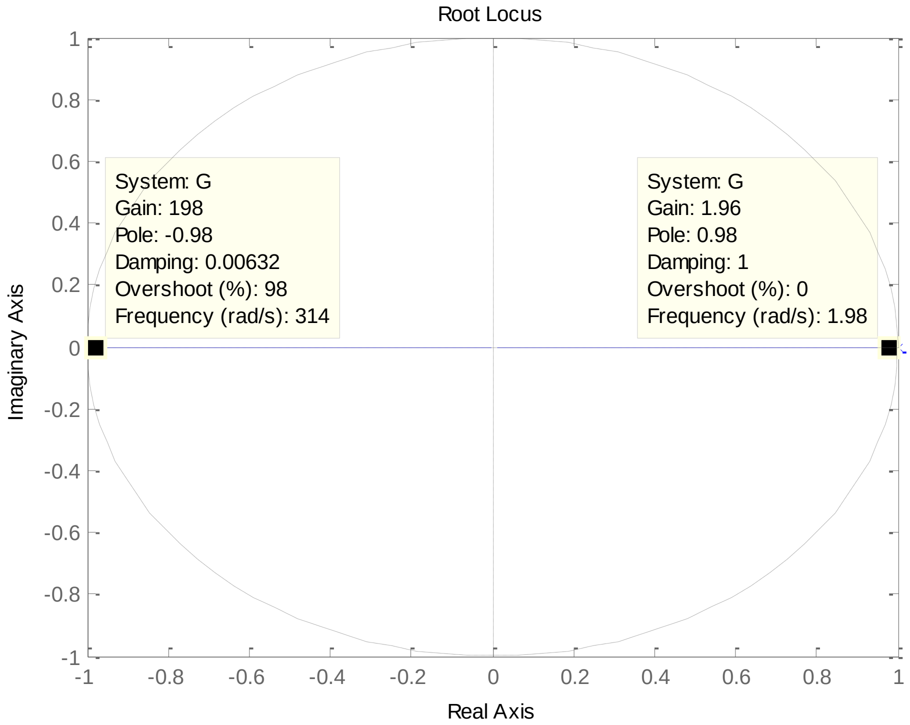

Figure 3

Figure 3 displays the new boundary values for the desired range of K values. From this root locus plot, the desired value of K can be given as a range of:

$$1.96 \leq K \leq 198$$

Range for K Satisfying Settling Time Specification

Since this range is a subset of the range developed for the stability and 0 steady state error specifications, this new range is the desired K values thus far. Any choice for the gain K in this range will satisfy the settling time requirement as well as the stability and 0 steady state error requirements. However, this range for the gain K does not take into account the maximum overshoot specification. As can be seen from the root locus in Figure 3, the upper bound (and a tremendous amount of high gains) have too high of an overshoot.

Overshoot Less than 5%

Similar to the first three specifications, the overshoot will be given as a range, and the range can be found using the same method – the root locus of the open loop discrete time system:

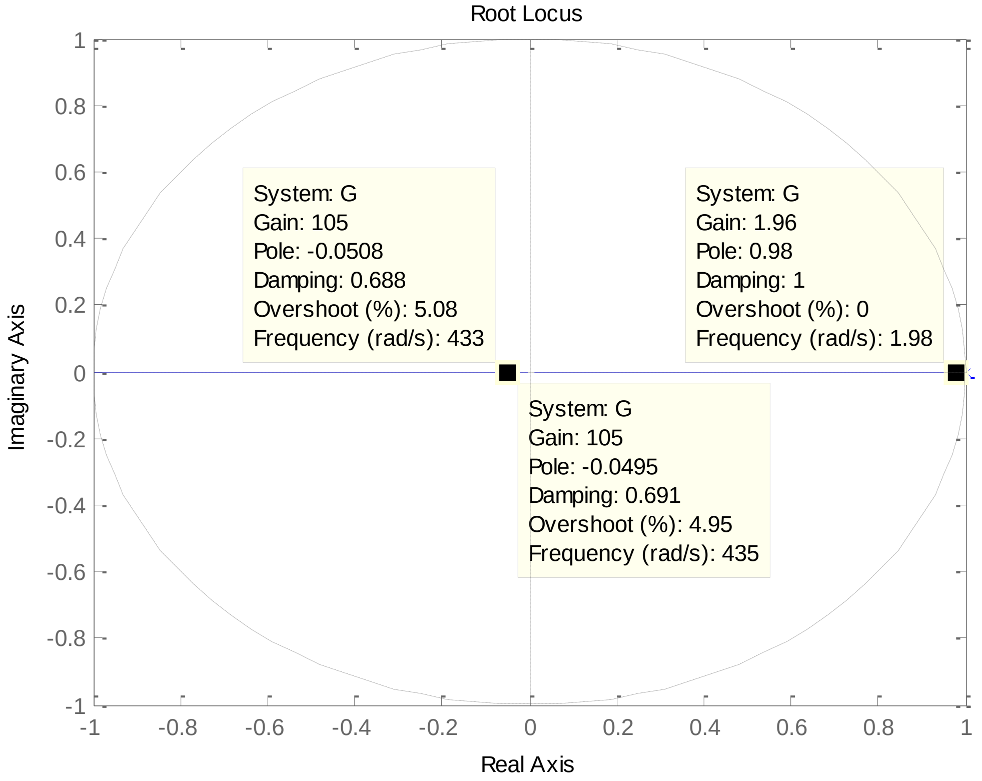

Figure 4

Figure 4 shows the boundary values satisfying the maximum overshoot specification. The two tags at the gain of 105 show overshoot percentages of 5.08 and 4.95. Therefore, it can be concluded that any gain less than 105 will meet the settling time specification. The lower bound will remain the same in order to maintain the satisfactory settling time behavior. The new range for the gain K is given by:

$$1.96 \leq K < 105$$

Range for K Meeting All Specifications

Since this range is a subset of the previously developed range, this new range gives the desired K values to meet all four specifications.

Controller Design Summary

The physical model originated as a continuous time transfer function given as:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{s}$$

Continuous Time Transfer Function (Continuous Time Plant)

Through a systematic discretization process, the model was converted to the discrete time transfer function given as:

$$G(z) = \frac{Y(z)}{U(z)} = \frac{.01}{z-1}$$

Discrete Time Transfer Function (Discrete Time Plant)

The specifications for the system were to have the system remain stable, have 0 steady state error, a setting time less than 2 seconds, and a maximum overshoot of less than 5%.

The specification of 0 steady state error was shown to be satisfied by use of the Final Value Theorem on the error of the discrete time transfer function:

$$e(\infty) = \lim_{z \to 1}(z-1)\ \frac{.01z(z-1)}{(z-1)(z-1+.01K)} = \lim_{z \to 1} \frac{.01z(z-1)}{(z-1+.01K)} = 0$$

Evaluation of the Final Value Theorem

Based on the root locus plots (shown in Figures 1 through 4) of the open loop discrete time system given by:

$$G(z)K(z) = \frac{.01K}{(z-1)}$$

Equation 15

A range for values of K that met the stability, 0 steady state error, settling time, and overshoot specifications was developed and is given as follows:

$$1.96 \le K < 105$$

Range for K Meeting All Specifications

This transfer function was tested in simulation using Simulink and in real-time using xPC Target and SCB to verify the specifications have been met.

Tests of Controller Design

The system was modeled in Simulink to test the specifications. The following block diagram was created to represent the system:

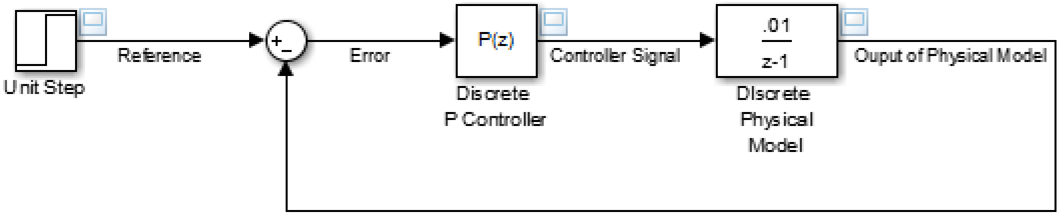

Figure 5

In all of the tests performed, the output of the physical model was plotted against the unit step reference. Also, the controller signal was plotted on a separate axis to confirm its behavior.

No Signal Check

The first test completed was a test on stability. For a K value of 0, the system will be unstable. However, the output of the physical model should read 0, since there is no controller signal entering its block when the K value is set to 0. The following plot shows the accuracy of this result:

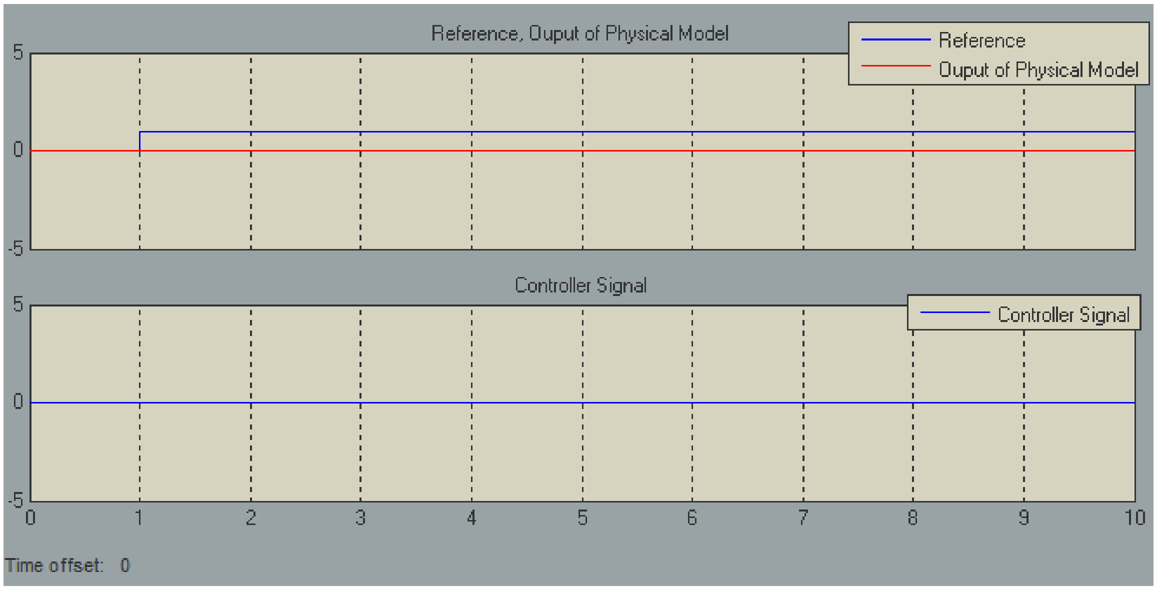

Figure 6

Figure 6 verifies that the controller signal and output of physical model are zero, as predicted.

Below Desired Range

The second test that was performed was a chosen value for the gain K that was below the desired range of:

$$1.96 \ \leq K \ < 105$$

A value of 1.0 was chosen for K. The system should be stable and meet the steady state error specification (all values of K should meet this specification as long as the system is stable) and the overshoot specification (this K value will give 0% overshoot). However, it should not meet the settling time specification. At 3 seconds, the output of the physical model will not reach an amplitude of .98:

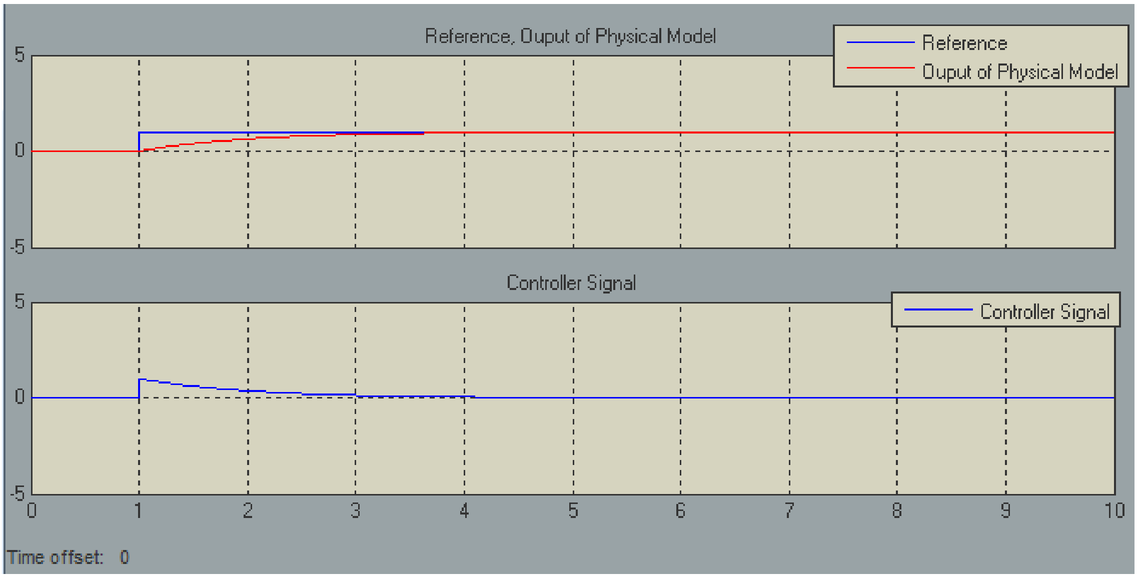

Figure 7

Figure 7 clearly shows the system is stable, there is 0 steady state error, and there exists no overshoot. The following plot is zoomed in around 3 seconds to visualize the settling time:

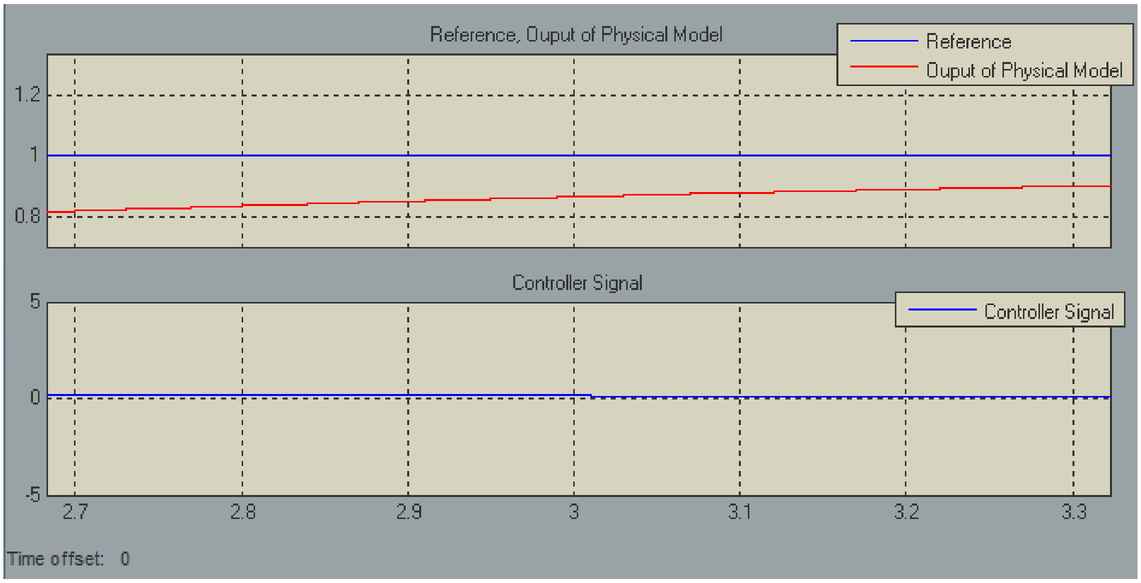

Figure 8

Figure 8 demonstrates that the settling time is not satisfied for this gain value – the output of the physical model does not reach an amplitude of .98 within 2 seconds of the unit step.

Within the Desired Range (All Specifications Met)

0% Overshoot

A series of tests were performed with a chosen K value within the desired range. Any of these K values should specify all of the given specifications. The first test in this series was conducted with a K value of 2.0. Similar to the K value of 1.0 in the previous test, this K value will have a 0% overshoot. The following two plots show that all three specifications have been met for this gain value:

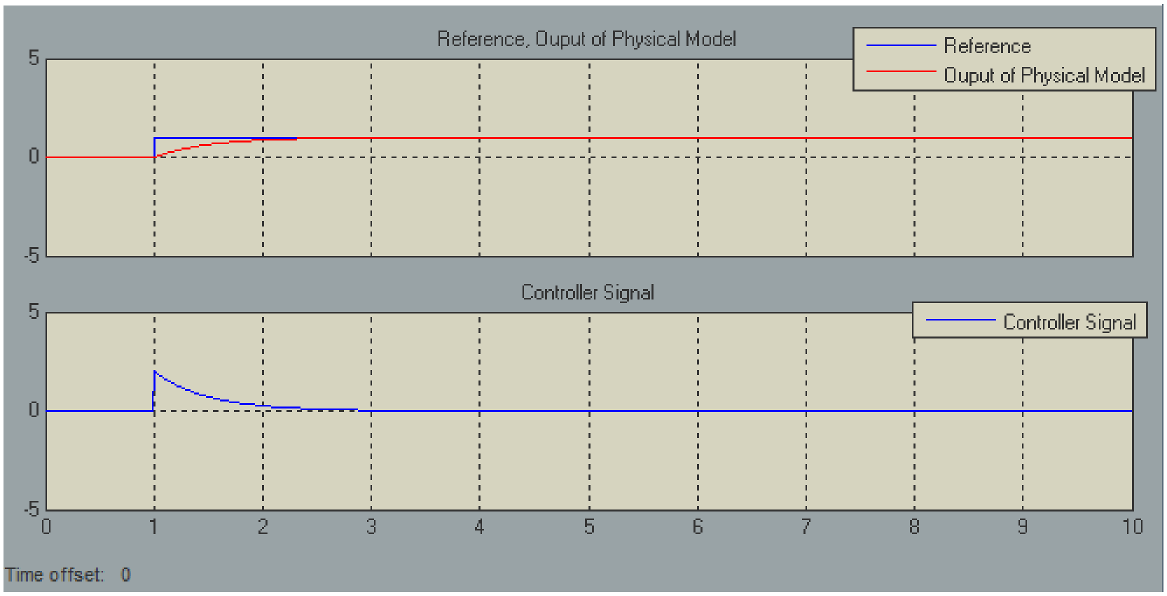

Figure 9

Similar to the gain value of 1 chosen for the previous test, Figure 9 shows the system is stable, there is 0 steady state error, and there is no overshoot. The following plot is zoomed in around 3 seconds to show that the settling time specification is indeed met:

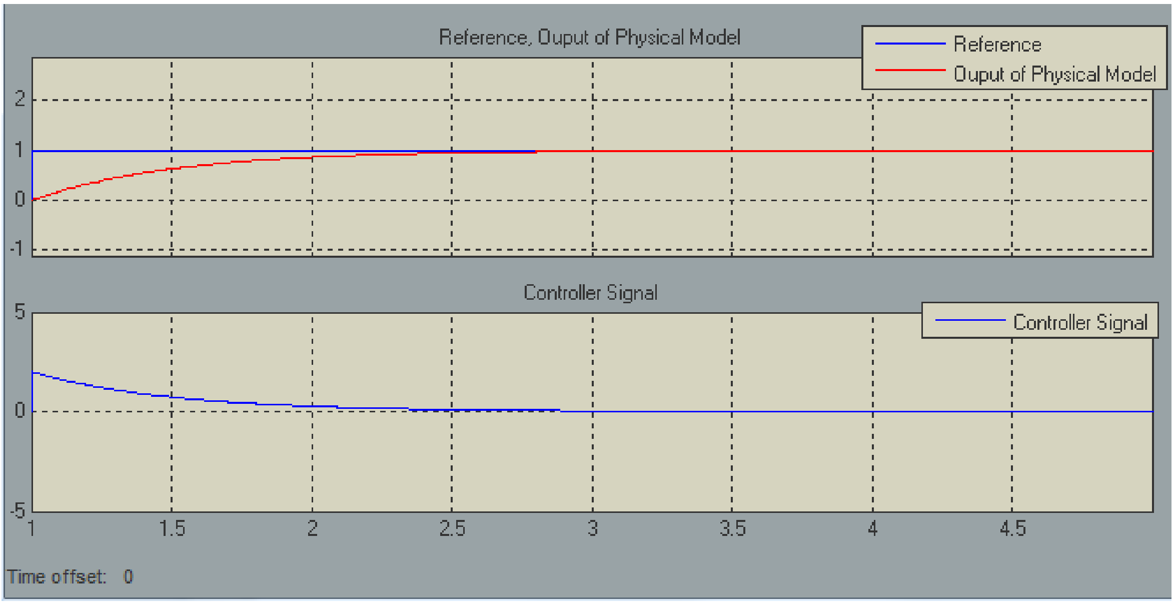

Figure 10

It is clear from the plot in Figure 10 that the settling time specification is well satisfied.

4% Overshoot

There exists a relationship between increasing overshoot and increasing gain. To visualize this, the gain value of 104 was chosen. This particular gain value will have a faster settling time than the previous test, but will have an overshoot of 4%. The following root locus plot in Figure 11 shows the overshoot will be exactly 4%:

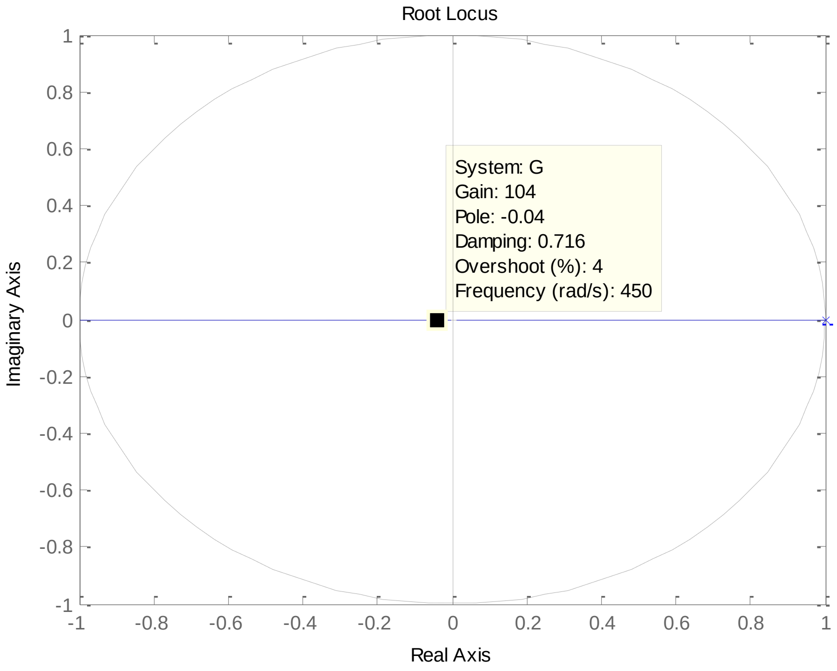

Figure 11

The following two plots show the simulation results for this gain value:

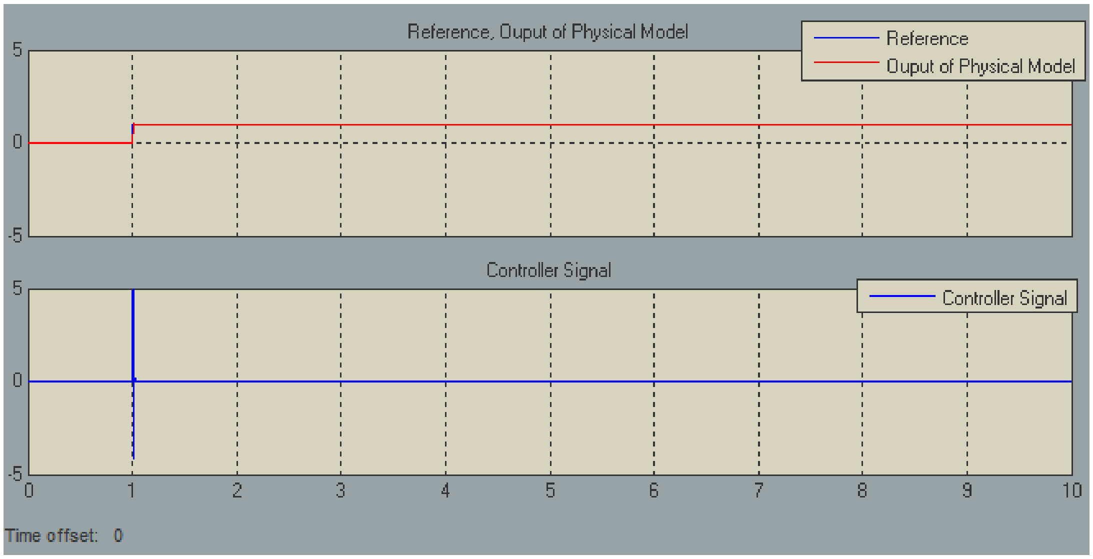

Figure 12

Figure 12 shows the stability and zero steady state error specifications are satisfied. The following plot is zoomed in around 1 second to see the 4% overshoot:

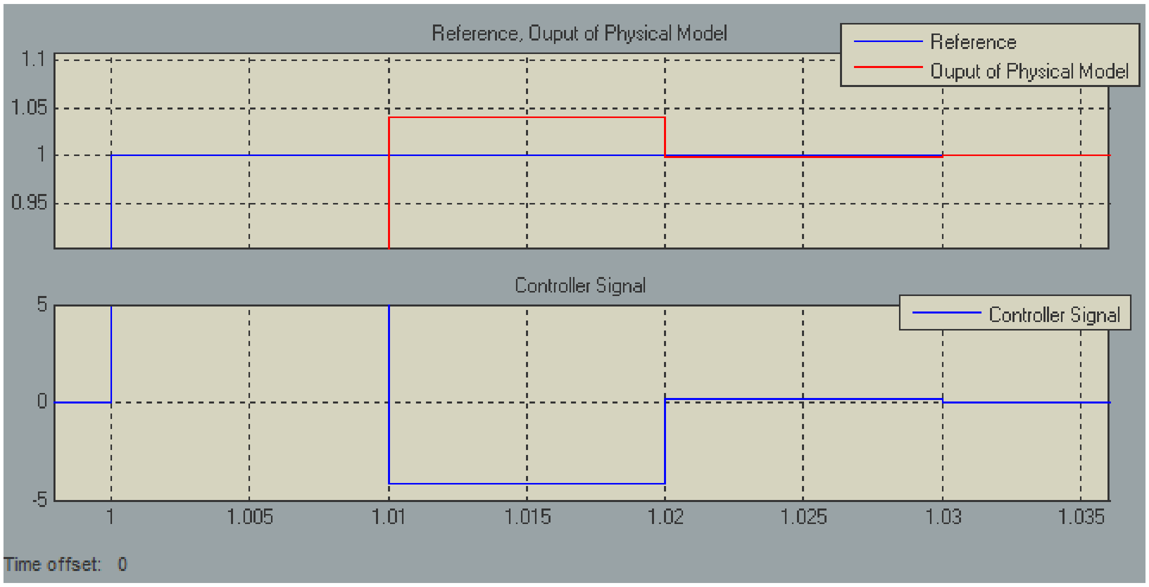

Figure 13

Figure 13 provides evidence that there is exactly 4% overshoot and the settling time is rapid.

Above the Desired Range

Settling Time Satisfied, 49.7% Overshoot

Another test performed was on a K value above the desired range. The chosen value of K was 150. This value will still satisfy the settling time and 0 steady state error specifications, but will have an overshoot 49.7%. Additionally, even though the settling time specification will be met, it will be slower than the settling time of gain value 104 in the previous test. For high gains, there is a tradeoff between settling time and rise time, with the cause being an increase in maximum overshoot. The following root locus plot in Figure 14 displays the relationship between the chosen gain value and maximum overshoot:

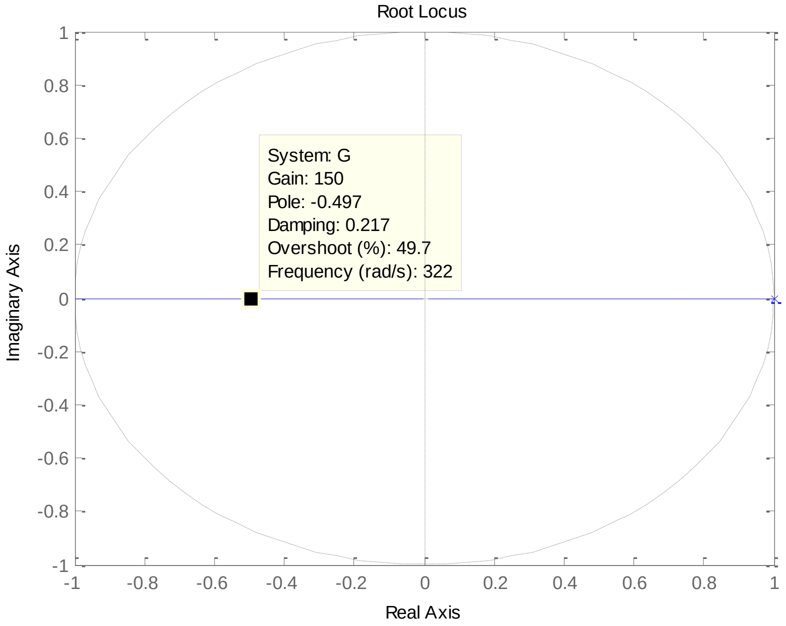

Figure 14

The following two plots show the simulation results for this gain value:

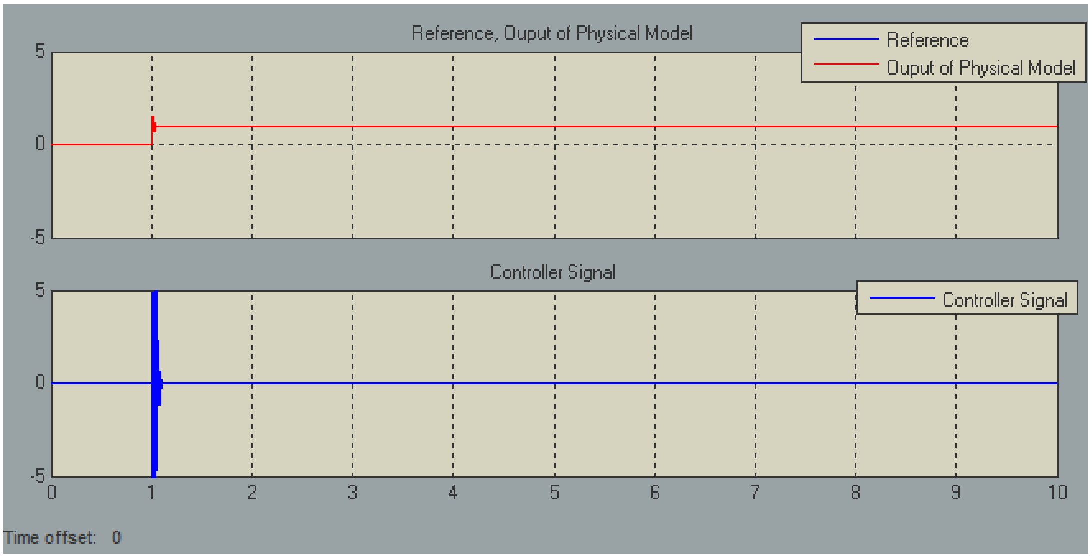

Figure 15

Figure 15 illustrates the stability and zero steady state error specifications are satisfied. The following plot is zoomed in around 1 second to see the 49.7% overshoot:

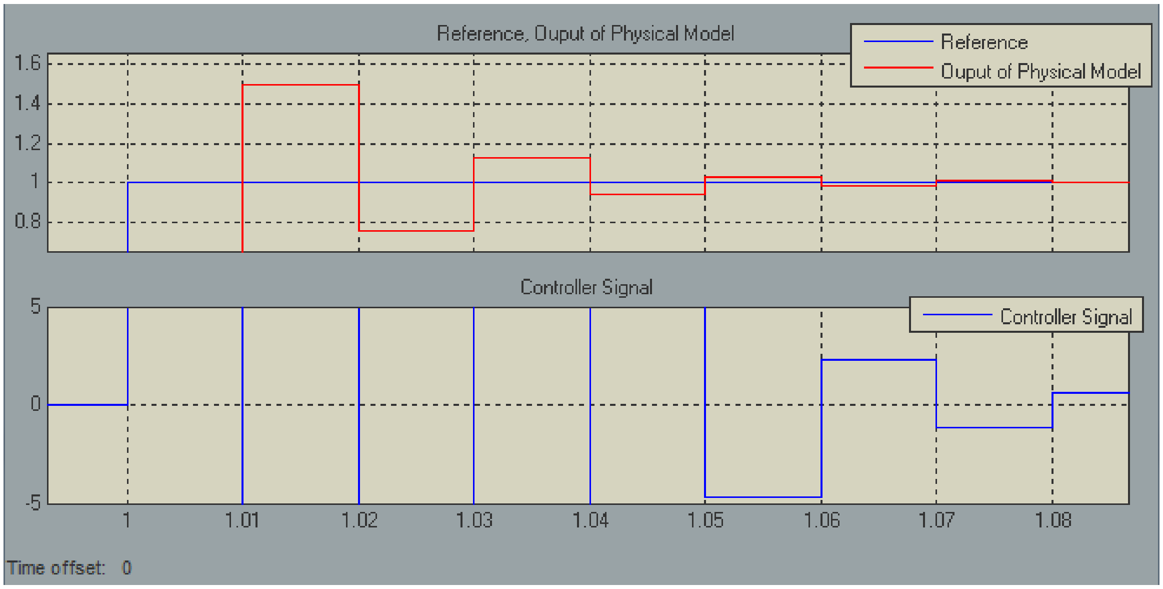

Figure 16

Although the settling time is well under 2 seconds, Figure 16 demonstrates that there is exactly 49.7% overshoot in the system.

Settling Time and Overshoot Undesirable (98.8% Overshoot)

In the final test, a gain value was chosen to be outside both desired ranges for the settling time and maximum overshoot. With this specific gain value, only the stability and 0 steady state error specifications should be met. A value of 199 will exhibit this behavior and will have an overshoot of 98.8%. The following root locus plot in Figure 17 exhibits the overshoot percentage for this gain value:

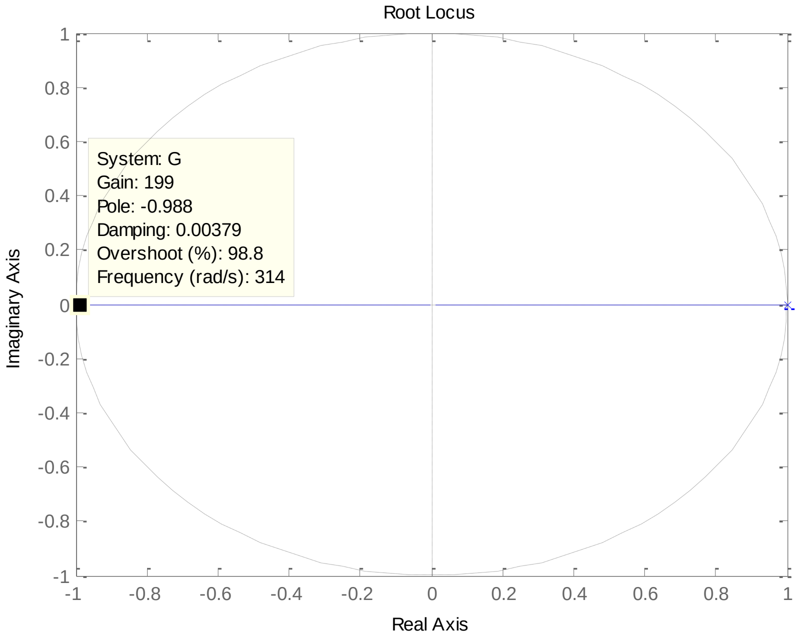

Figure 17

The following two plots show the simulation results for this gain value:

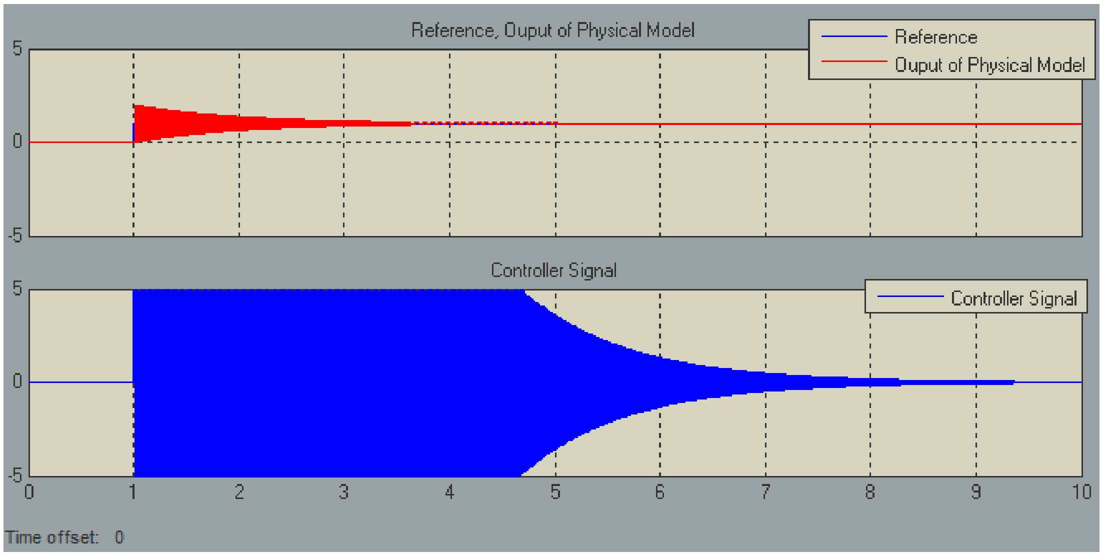

Figure 18

Figure 18 shows that the system is still stable and will have zero steady state error. This final simulation confirms that the system will have zero steady state error for all K values within the desired range. Clearly, the settling time specification is not met for this gain value. In fact, it is about three times slower (6 seconds) than what it needs to be (2 seconds). The following plot is zoomed in around 1 second to visualize the 98.8 overshoot:

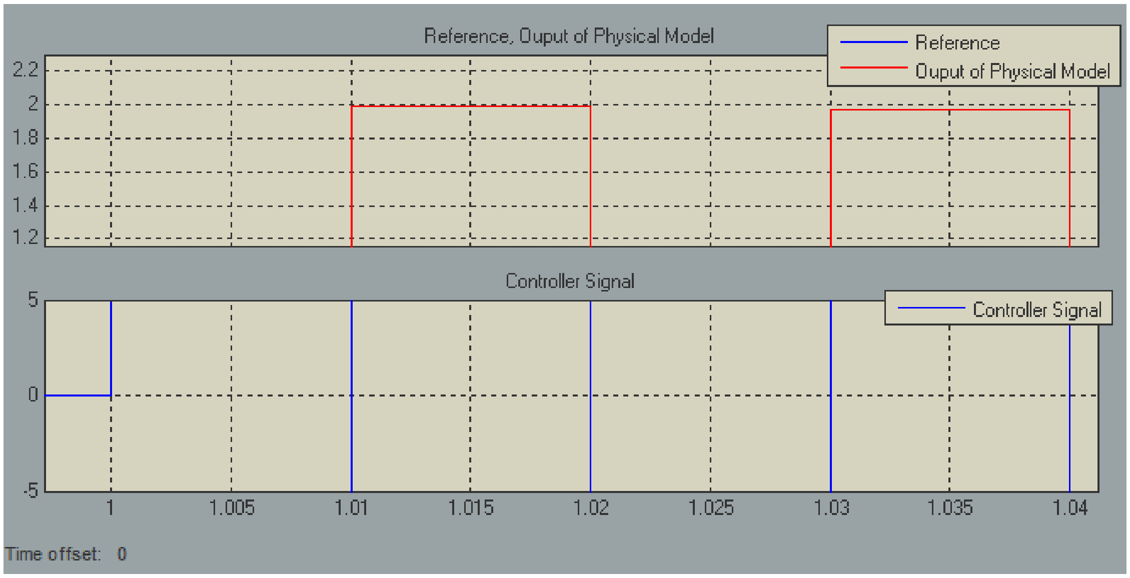

Figure 19

Figure 19 displays the 98.8% overshoot. The system is behaving as predicted.

Since the closed behavior has been satisfied, the system is now ready for real-time testing using xPC Target and Stamped Circuit Board (SCB).

Real-Time Tests of Controller Design

The following block diagram was created to represent the system in real-time:

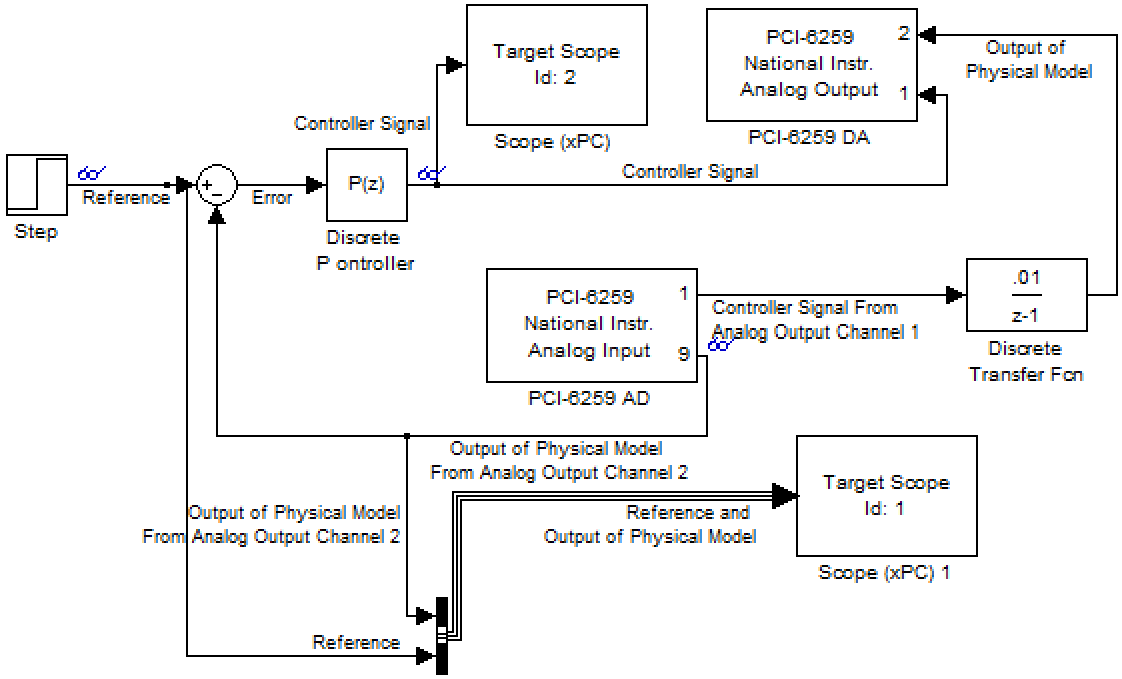

Figure 20

The signal begins with the familiar reference - a unit step. The signal is fed through the discrete proportional controller and sent out of the computer through the analog output channel 1. Since this is simply a simulation of a real world system, the signal will be directly sent back into the computer through analog input channel 1. There is no middle step between analog output channel 1 and analog input channel 1.

In actual real-time systems, there are a few middle steps. After leaving through the analog output, there is often a physical plant, as well as sensors, that the signal would process through before entering back into the computer through the analog input.

To simulate that event, the signal received by analog input channel 1 is sent through the physical model (discrete time transfer function) $G(z)$. This signal is directed out of the computer again by analog output channel 2 to only be brought right back into the computer by analog input channel 9. Similar to the first analog output/input scenario, there is no middle step between the analog input/output. Finally, the signal is compared with the reference to create the error signal and completing the loop.

It is important to note that the analog input/analog outputs were built in this model in a “backwards” sense when compared to a real world system. Typically, signals from the plant are received from the analog output and sent to the analog input. For this block diagram, the signal going to $G(z)$ originates from an analog input and the signal leaving $G(z)$ goes into the analog output. Again, this is backwards from a real world system. However, the backwardness is a consequence of having the "real world model" be in the computer and not outside of it. Therefore, the "real world model" needs analog inputs sending it the signal and analog outputs receiving its signal.

Given that the analog outputs/analog inputs are just simulations of what would happen with a real physical feedback loop, it is hypothesized that the behavior of the system would be the same as in the case where the analog input/output blocks are not present in the system. Any discrepancies in the results can be attributed to having a not perfect SCB wiring, (a wire is faulty, heating up, etc.) and signal noise. Because of the signal noise, there will be some error when the system reaches steady state.

The specifications for the real-time system were validated in the same process as the simulated system. It is important to note that the real-time system can never truly satisfy the specification of zero steady state error. This is due to the presence of the signal noise originating from the SCB and flowing through the model via Analog Output/Input blocks. However, this noise signal can be handled very well by the controller for reasonable gain. For example, a gain value of 1.0 at steady state produces the following plot:

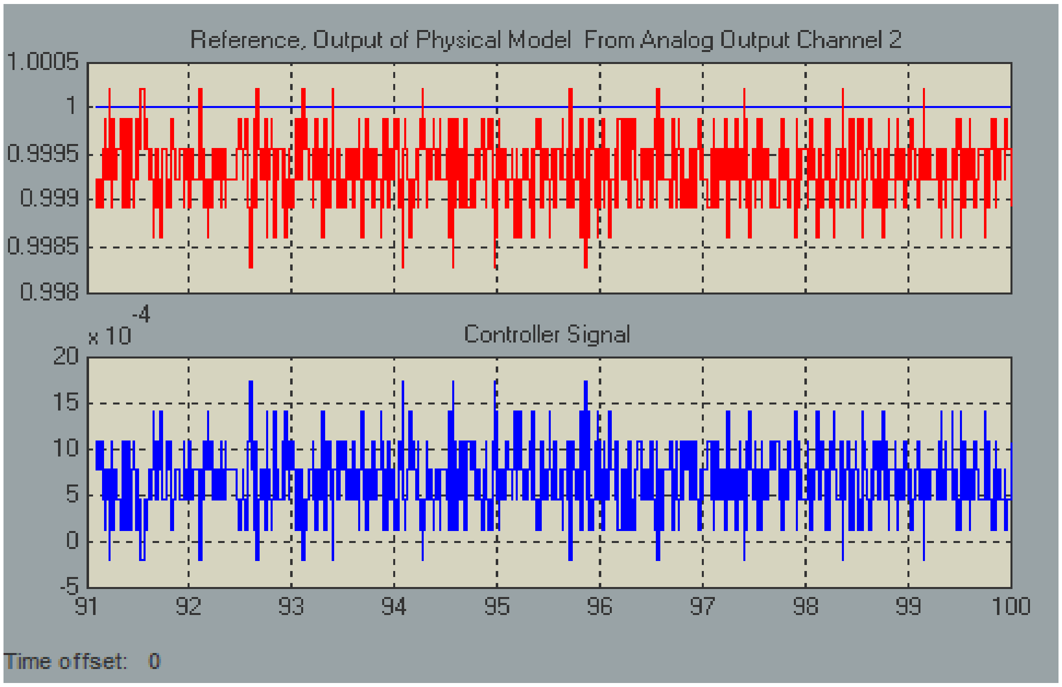

Figure 21

Figure 21 shows the range for the noise signal is smaller than .0025. Thus, it can be considered negligible. Therefore, any gain values producing a steady state value in this range can be considered the new specification for steady state error. It is expected that this noise signal will amplify as the controller gain increases. Therefore, it is predicted that there will be a shortened desired range for K to meet the maximum overshoot specification.

Additionally, to prevent any damage to the equipment, the controller signal was limited to an output of +/- 10. This gives a maximum value for K, which was experimentally found to be 61.64. This immediately creates a new desired range for K and is given by:

$$1.96 \le K \le 61.64$$

Real-Time Range for K

The following plot shows a gain value of 100, which is outside of this new range:

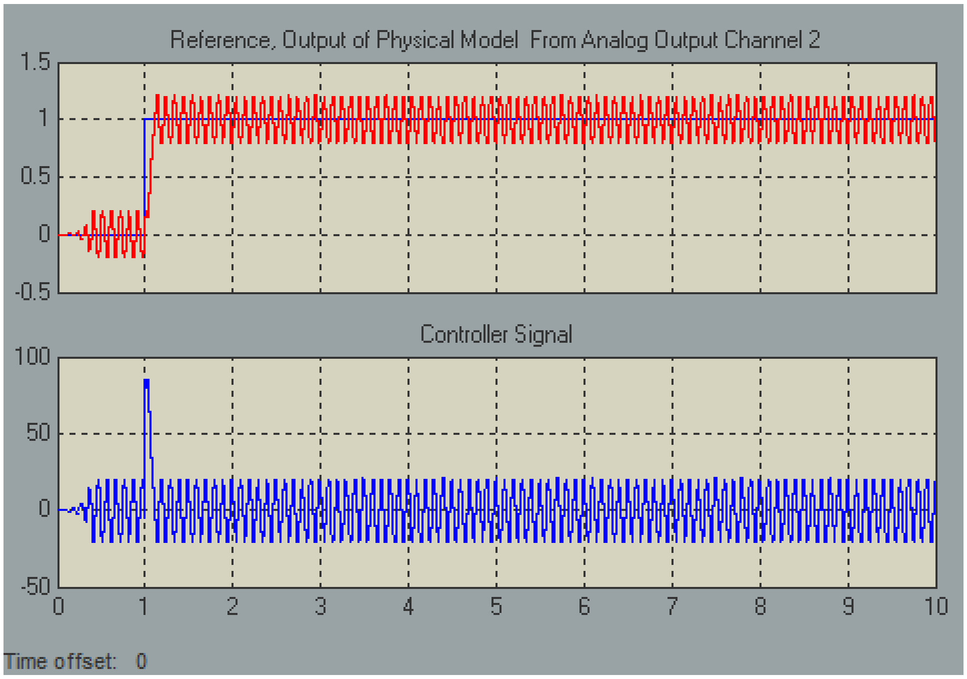

Figure 22

In the simulated case, the system reached steady state within a tenth of a second after the step input. However, Figure 22 shows that the real-time system clearly portrays different characteristics. This is caused by a saturation of the controller signal.

No Signal Check

To make sure the system is operating as it should, the real-time system was subjected to a controller signal of 0. In this situation, the output of the physical model and controller signal should both read zero (not taking into account the circuit noise). The following plot serves to verify this fact:

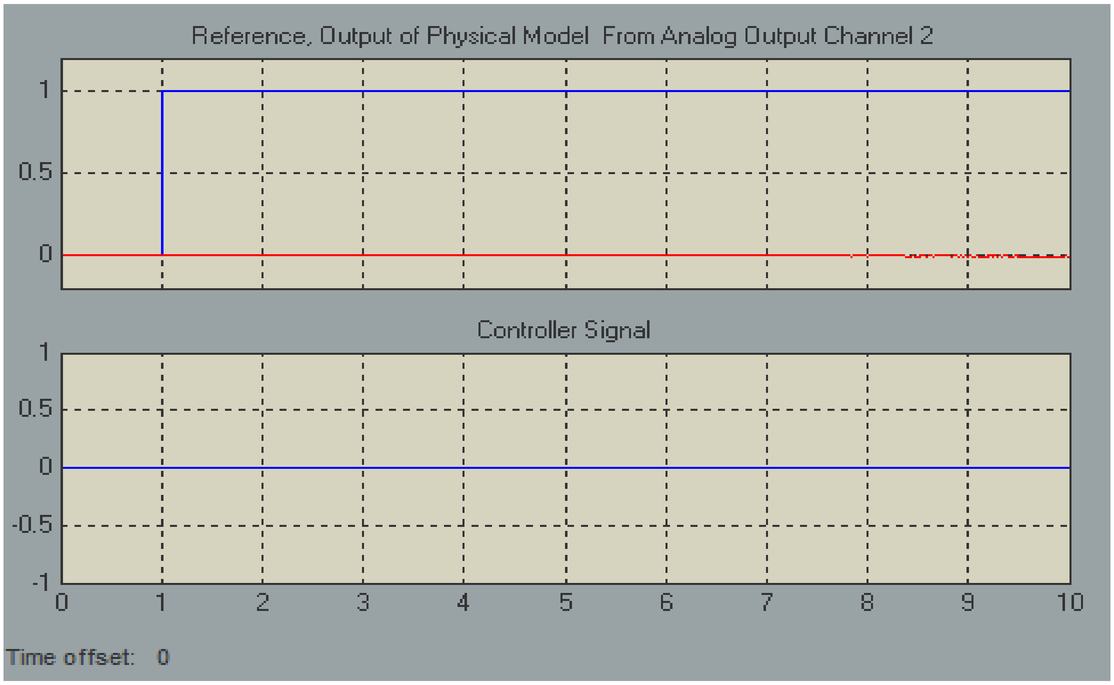

Figure 23

Figure 23 show's that the controller signal is indeed 0. However, the output of the physical model picks up a small amount of circuit noise input, which is evidenced by the fluctuation from zero in the time interval from 8 to 10 seconds.

Below the Desired Range

As for the simulated system, a gain value for K was chosen to be 1.0. With this gain value, the settling time specification will not be met. There will not be any overshoot and the system will be stable with zero steady state error:

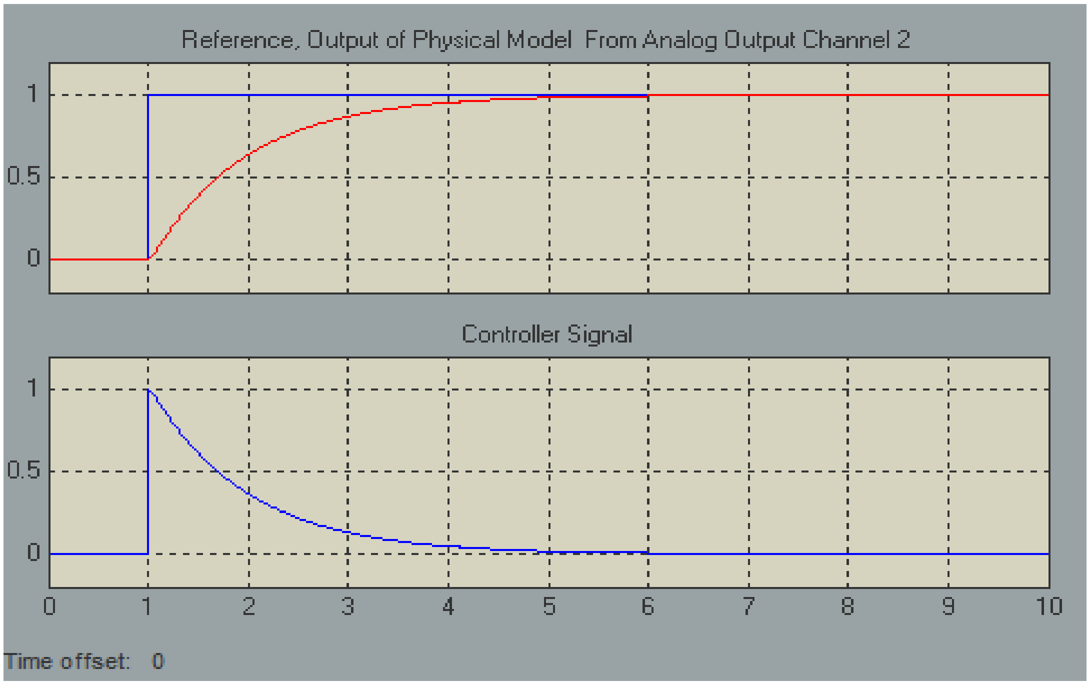

Figure 24

Similar to the simulation results in Figure 7, Figure 24 shows the stability, 0 steady state error, and maximum overshoot specifications are satisfied while the settling time is not.

The following plot is zoomed in around three seconds:

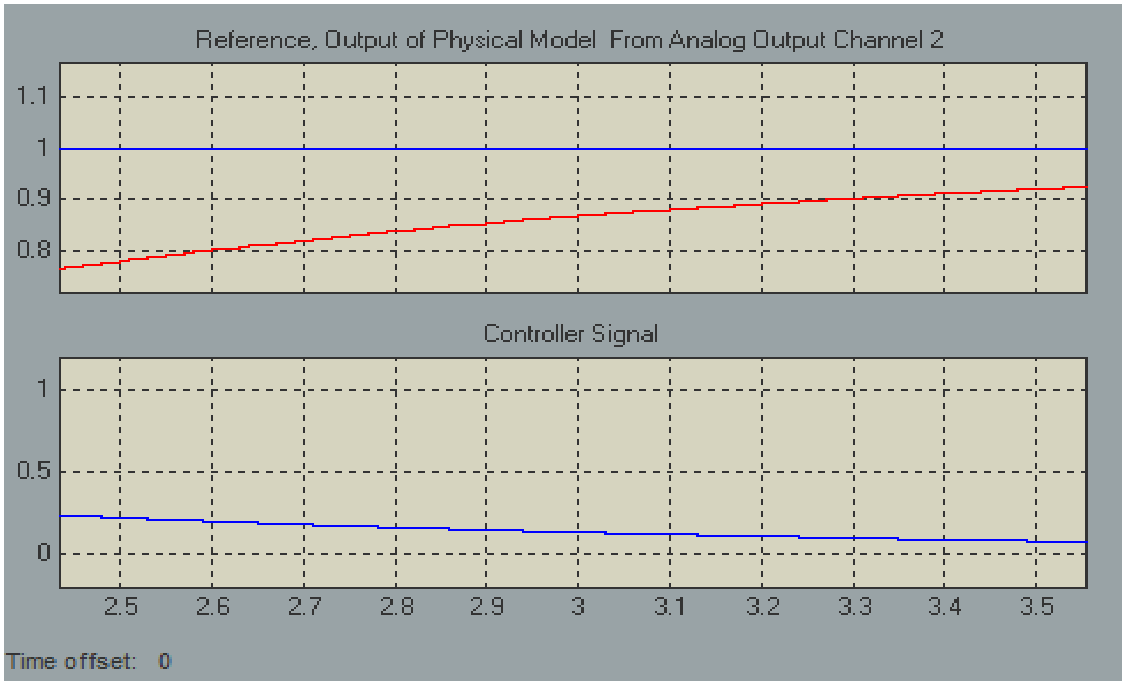

Figure 25

From Figure 25, it is clear that the system does not reach .98 of its final value within two seconds after the reference input. So far the real-time system is in complete agreement with the theoretical results.

Within the Desired Range (All Specifications Met)

0% Overshoot

In the simulated case, a gain value for K was chosen to be 2.0. That same value was used in the real-time system. The simulated system met all four specifications and the same result is expected for the real-time system:

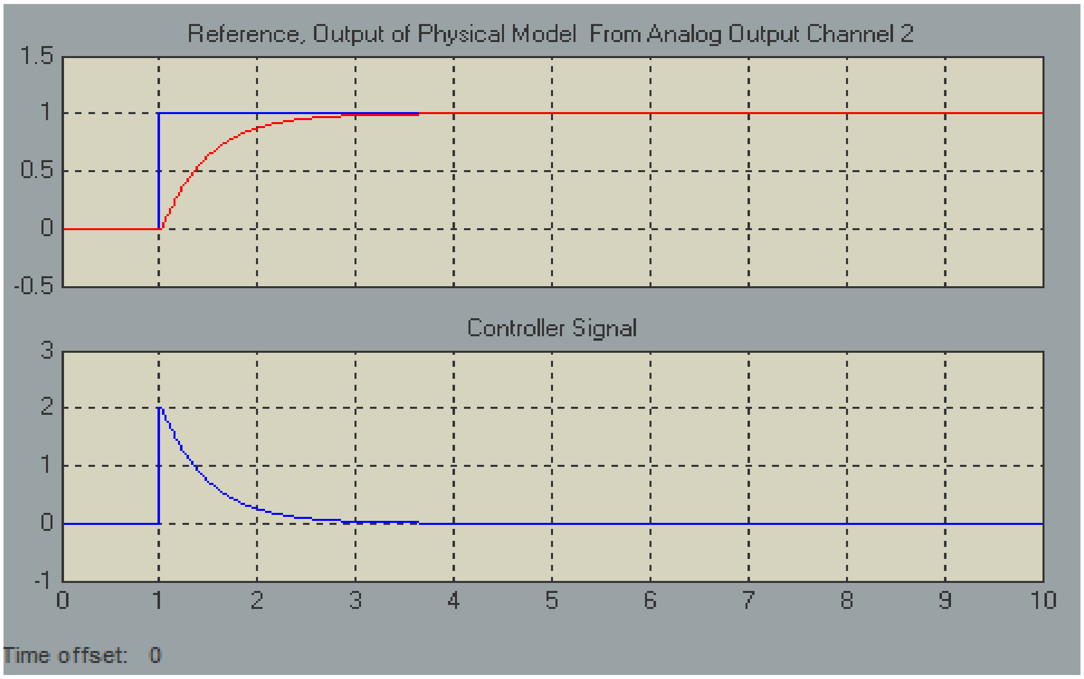

Figure 26

The real-time results in Figure 26 perfectly correspond to the simulated results in Figure 9. The stability, 0 steady state error, and maximum overshoot specifications are all satisfied.

The following plot is zoomed in around three seconds:

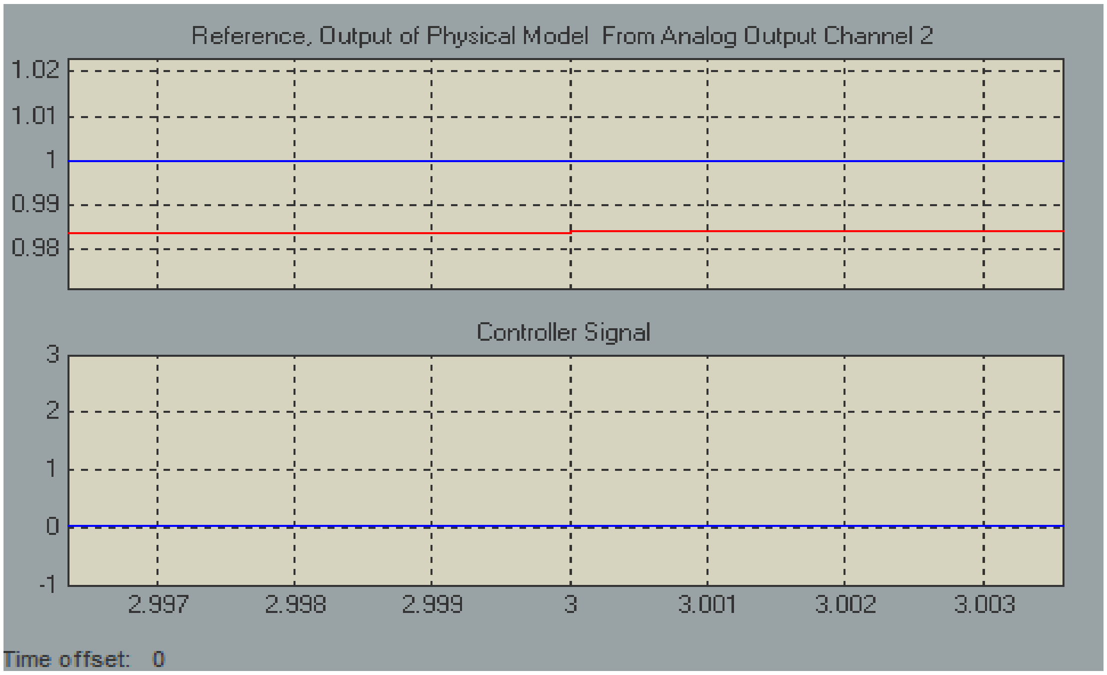

Figure 27

From Figure 27, it is clear that the settling time specification is satisfied – the system reaches .98 of its final value within two seconds of the unit step input.

Determining New Range for K

Since an increasing gain is expected to respond poorly to the circuit noise signal, a new range for K satisfying the maximum overshoot specification is in order. For a K value of 25, the system has the following characteristics:

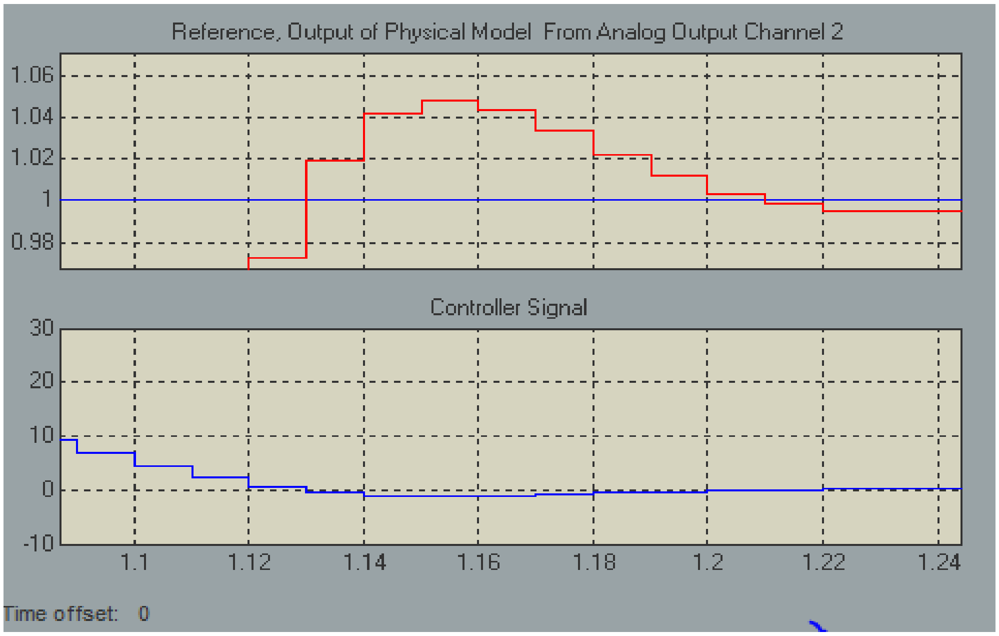

Figure 28

Figure 28 shows the output of the physical model barely meets the overshoot specification. Additionally, this gain value produces a steady state value within the .0025 range specified earlier. Hence, it can be considered to meet the stability and zero steady state error specifications:

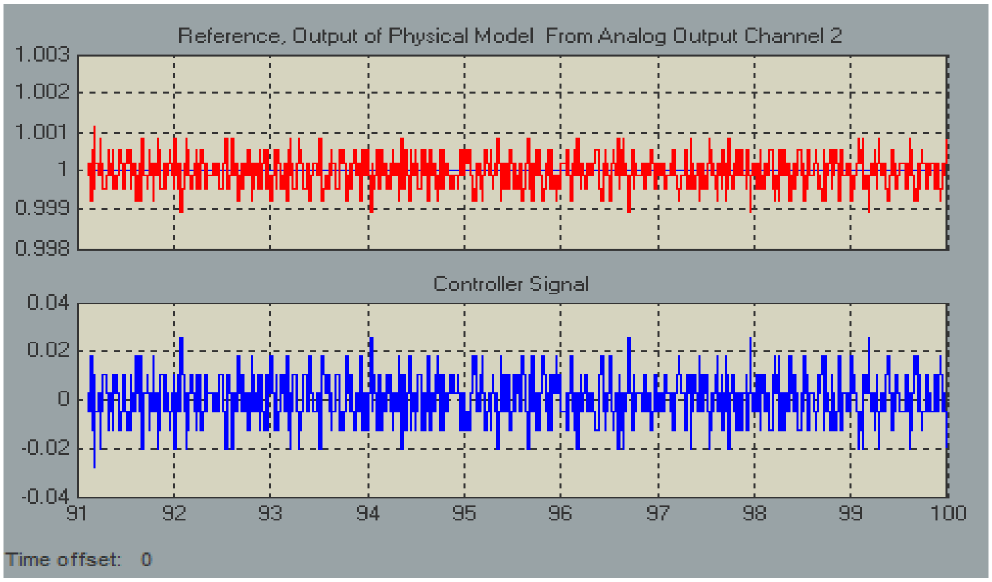

Figure 29

Summary

From the results shown, it can be seen that a continuous time controller of the form:

$$G(s) = \frac{1}{s}$$

Continuous Time Controller (Continuous Time Plant)

Was appropriately discretized into:

$$G(z) = \frac{.01}{z - 1}$$

Discrete Time Controller (Discrete Time Plant)

A proportional controller (K) was then adequately designed to have the discrete time system meet the following specifications:

- The system should be stable
- 0 steady state error to a unit step input
- A setting time of less than 2 seconds
- And an overshoot less than 5%

The range for K meeting all the specifications was found using root locus methods to be:

$$1.96 \ \leq K \ < 105$$

Simulated Desired Range for K Meeting All Specifications

Before implementing the controller on the real-time system, the controller was tested in Simulink. The results validated the range given for K and the controller was then tested in real-time.

It was hypothesized and confirmed that a new range for K would need to be constructed for the real-time system. This was due to the presence of circuit noise and a limit on controller output. Since the proportional controller reads this signal noise as an error, the output of the physical model would portray different characteristics for high gains when compared to the simulated system. Also, to prevent damage to lab equipment, the controller was limited to an output of +/- 10. The new range for the gain K was experimentally found to be:

$$1.96 \ \leq K \ \leq 25$$

Experimentally Determined Range for K Meeting All Specifications

From this new range, an ideal controller can be selected. For high gains, there is a natural tradeoff between settling time and peak time, and since peak time is directly related to overshoot, there exists a relationship between settling time and maximum overshoot. Small gain values possess little to no overshoot but give long settling times. However, large gain values can give a variety of results. A large gain value can give fast settling times with low overshoot, but they can also give long settling times with large or maximum overshoot. From these relationships, there are some gain values that exhibit an ideal and balanced behavior among all of the specifications. A gain value of 18 displayed quality settling time and overshoot characteristics, which is shown in the following two plots:

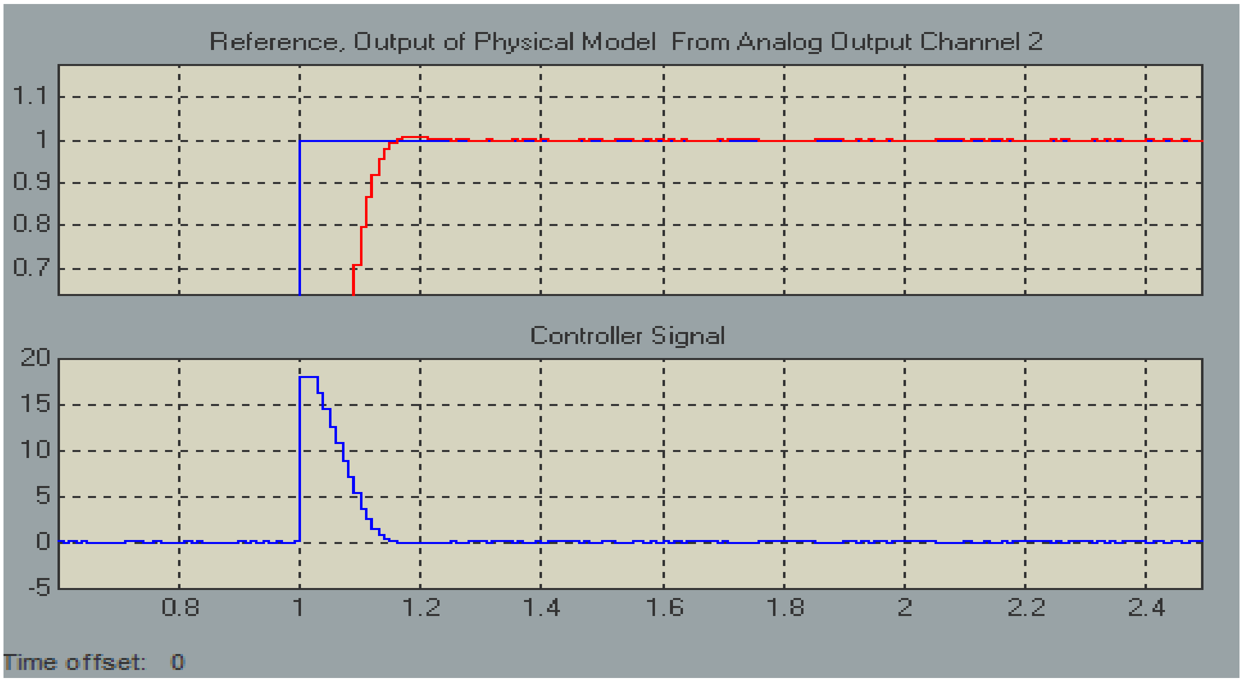

Figure 30

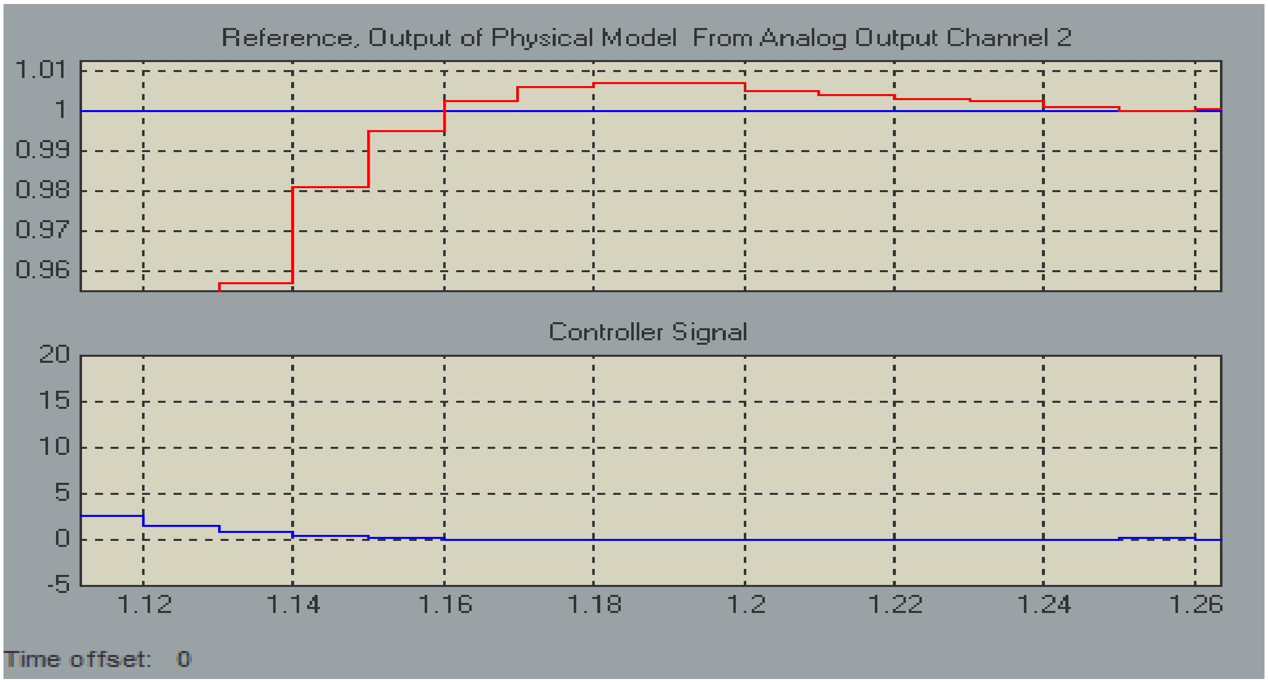

Figure 31

The previous two plots in Figures 30 and 31 show that the settling time is about 1.15 seconds while the maximum overshoot is approximately .07%. Also, the steady state response is within the .0025 range for zero steady state error:

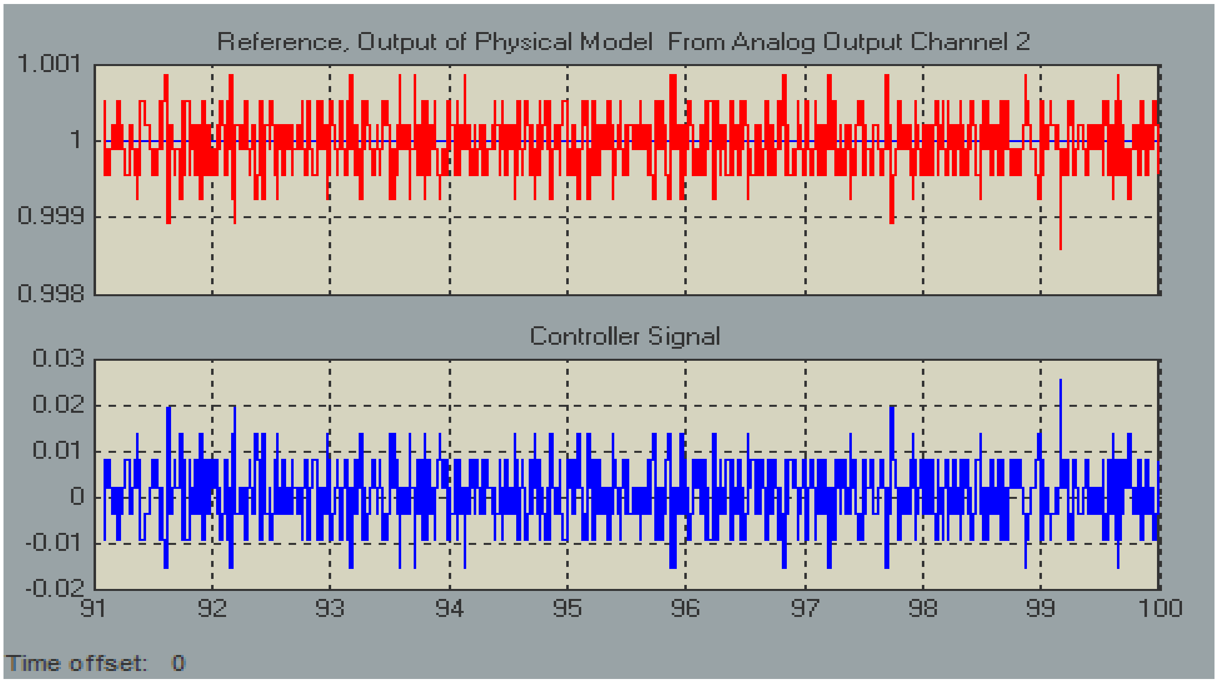

Figure 32

Therefore, the open loop discrete time system that meets the specifications and gives ideal real-time behavior is:

$$G(z)K = \frac{.01\,(18)}{z-1} = \frac{.18}{z-1}$$